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WHAT IS CLAIMED IS:

1. A die seal structure for a semiconductor die having a substrate comprising:

an elongate region electrically isolated from the remainder of the substrate extending around a major portion of the periphery of the substrate and having a gap between ends of the elongate region along a minor portion of the periphery; and

a conductive seal ring extending around the entire periphery of the die in contact with the die at said elongate region and said gap to provide a limited electrical connection between the ring and the substrate at said gap.

2. The structure of claim 1 wherein the substrate has a first conductivity type, and wherein the elongate region comprises an elongate well region of a second conductivity type different from the conductivity of the first conductivity type.

3. The structure of claim 2 wherein the first conductivity type is p-type and the second conductivity type is n-type.

4. The structure of claim 2 wherein the first conductivity type is n-type and the second conductivity type is p-type.

5. The structure of claim 1 wherein the elongate region comprises an elongate dielectric region between the seal ring and the substrate.

6. The structure of claim 1 wherein the seal ring only electrically contacts the substrate of the semiconductor die at the gap.

7. The structure of claim 1 wherein the substrate is formed of silicon.

8. The structure of claim 1 wherein the conductive seal ring comprises a multilayer structure of alternating conducting and insulating layers, and wherein vias are formed in the insulating layers.

9. A method of sealing a semiconductor die having a substrate of a first conductivity type, comprising:

forming an elongate well region of a second conductivity type opposite from the first conductivity type extending around a major portion of the periphery of the

substrate and having a gap between ends of the well region at a minor portion of the periphery; and

placing a conductive seal ring extending around the entire periphery of the die in contact with said well region and said gap to provide limited electrical contact between the ring and the substrate of said first conductivity type at said gap.

10. The method of claim 9 wherein the substrate of the semiconductor die has an n-type conductivity and wherein said forming an elongate well region of a second conductivity type step includes forming an elongate well region of a p-type conductivity.

11. The method of claim 9 wherein the substrate of the semiconductor die an n-type conductivity and wherein said forming an elongate well region of a second conductivity type step includes forming an elongate well region of a p-type conductivity.

12. The method of claim 9 wherein the substrate of the semiconductor die is formed of silicon.

13. The method of claim 9 wherein said placing step includes sequentially forming a multiplicity of alternating conductive and insulative layers overlying one another, and forming vias in the insulating layers.

Subject

14. A die seal structure for a semiconductor die having a substrate of a first conductivity type, comprising:

an elongate well region of a second conductivity type opposite from the first conductivity type extending around a major portion of the periphery of the substrate and having a gap between the ends of the elongate region along a minor portion of the periphery; and

a conductive seal ring extending around the entire periphery of the die in contact with the die at said elongate well region and said gap to provide a limited electrical connection between the ring and the substrate of said first conductivity type at said gap.

15. The structure of claim 14 wherein the first conductivity type is p-type and the second conductivity type is n-type.

16. The structure of claim 14 wherein the first conductivity type is n type and the second conductivity type is p type.

17. The structure of claim 14 wherein the conductive seal ring comprises a multilayer structure of alternating conducting and insulating layers, and wherein vias are formed in the insulating layers.

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18. A semiconductor device comprising:

a. a die including a substrate;

b. a die seal structure on the substrate, the structure comprising:

an elongate region electrically isolated from the remainder of the substrate extending around a major portion of the periphery of the substrate and having a gap between ends of the elongate region along a minor portion of the periphery; and

a conductive seal ring extending around the entire periphery of the die in contact with the die at said elongate region and said gap to provide a limited electrical connection between the ring and the substrate at said gap.

19. The structure of claim 18 wherein the substrate has a first conductivity type, and wherein the elongate region comprises an elongate well region of a second conductivity type different from the conductivity of the first conductivity type.

20. The structure of claim 18 wherein the first conductivity type is p-type and the second conductivity type is n-type.

21. The structure of claim 18 wherein the first conductivity type is n-type and the second conductivity type is p-type.

22. The structure of claim 18 wherein the elongate region comprises an elongate dielectric region between the seal ring and the substrate.

23. The structure of claim 18 wherein the seal ring only electrically contacts the substrate of the semiconductor die at the gap.

24. The structure of claim 18 wherein the substrate is formed of silicon.

25. The structure of claim 18 wherein the conductive seal ring comprises a multilayer structure of alternating conducting and insulating layers, and wherein vias are formed in the insulating layers.

26. The structure of claim 18 wherein the elongate region is isolated by oxide.

27. The structure of claim 26 wherein the conductive seal ring is connected to the substrate by a metal stub.